AMENDMENTS TO THE CLAIMS

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

1. (CURRENTLY AMENDED) An apparatus comprising:

a Darlington transistor pair configured to generate an output signal at an output node in response to an input signal received through an input node; ~~and~~

a bias circuit coupled between an output transistor of said Darlington transistor pair and said input node, said bias circuit comprising (a) a bias transistor, (b) a bypass capacitor, and (c) a resistor connected between a base of said bias transistor and base of said output transistor; and

an isolation resistor coupled between said input node and a collector of said bias transistor, said isolation resistor configured to improve low frequency radio frequency (RF) response.

2. (ORIGINAL) The apparatus according to claim 1, wherein said resistor comprises a choke resistor.

3. (ORIGINAL) The apparatus according to claim 1, wherein said bias circuit further comprises:

an emitter bias resistor configured to set a class A, AB, B or other quiescent bias state.

4. (ORIGINAL) The apparatus according to claim 2, further comprising:

a low noise filter implementation comprising at least one choke inductor and at least one bypass capacitor.

5. (CURRENTLY AMENDED) The apparatus according to claim 2, further comprising:

an ~~isolation~~ bias resistor coupled between ~~said input node and~~ a collector of said bias transistor~~, said isolation resistor configured to improve low frequency radio frequency (RF) response~~ and said output node, said bias resistor configured to set the bias current of said apparatus.

6. (ORIGINAL) The apparatus according to claim 1, wherein said apparatus is monolithically integrated.

7. (ORIGINAL) The apparatus according to claim 1, wherein said apparatus is packaged in a 3-terminal package.

8. (ORIGINAL) The apparatus according to claim 1, wherein said apparatus comprises a self-bias Darlington amplifier.

9. (ORIGINAL) The apparatus according to claim 1, wherein said apparatus is tolerant to supply and temperature variations.

10. (ORIGINAL) The apparatus according to claim 1, wherein said apparatus enables dynamic bias operation.

11. (ORIGINAL) The apparatus according to claim 1, wherein said apparatus is implemented using 3.3V SiGe HBT and Si BJT Darlington gain blocks.

12. (ORIGINAL) The apparatus according to claim 1, wherein said Darlington transistor pair comprises a distributed Darlington amplifier.

13. (CURRENTLY AMENDED) An apparatus comprising:

a Darlington transistor pair configured to generate an output signal at an output node in response to an input signal received through an input node; ~~and~~

means for coupling between an output transistor of said Darlington transistor pair and said input node comprising (a) a bias transistor, (b) a bypass capacitor, and (c) a resistor connected between a base of said bias transistor and base of said output transistor; and

means for implementing an isolation resistor coupled between said input node and a collector of said bias transistor, said isolation resistor configured to improve low frequency radio frequency (RF) response.

14. (CURRENTLY AMENDED) A method for self-biasing a Darlington amplifier comprising the steps of:

(A) implementing a Darlington transistor pair configured to generate an output signal at an output node in response to an input signal received through an input node; ~~and~~

(B) coupling a bias circuit between an output transistor of said Darlington transistor pair and said input node, said bias circuit comprising (a) a bias transistor, (b) a bypass capacitor, and (c) a resistor connected between a base of said bias transistor and base of said output transistor; and

(C) coupling an isolation resistor between said input node and a collector of said bias transistor, said isolation resistor configured to improve low frequency radio frequency (RF) response.

15. (ORIGINAL) The method according to claim 14, wherein said resistor comprises a choke resistor.

16. (ORIGINAL) The method according to claim 14, wherein said bias circuit further comprises:

an emitter bias resistor configured to set a class A, AB, B or other quiescent bias state.

17. (CURRENTLY AMENDED) The method according to claim 14, further comprising:

implementing a low noise filter ~~implementation~~ comprising at least one choke inductor and at least one bypass capacitor.

18. (CURRENTLY AMENDED) The method according to claim 14, further comprising:

implementing ~~an isolation~~ a bias feedback resistor coupled between said ~~input node and a~~ collector of said bias transistor~~, said isolation resistor configured to improve low frequency radio frequency (RF) response~~ and said output node.

19. (CURRENTLY AMENDED) The method according to claim 14 ~~1~~, wherein said Darlington transistor pair and said bias circuit are monolithically integrated.

20. (CURRENTLY AMENDED) The method according to claim 14 ~~1~~, wherein said Darlington transistor pair and said bias circuit are packaged in a 3-terminal package.

21. (NEW) An apparatus comprising:

a Darlington transistor pair configured to generate an output signal at an output node in response to an input signal received through an input node;

a bias circuit coupled between an output transistor of said Darlington transistor pair and said input node, said bias circuit comprising (a) a bias transistor, (b) a bypass capacitor, and (c) a choke resistor connected between a base of said bias transistor and base of said output transistor; and

an isolation resistor coupled between said input node and a collector of said bias transistor, said isolation resistor configured to improve low frequency radio frequency (RF) response.

22. (NEW) An apparatus comprising:

a Darlington transistor pair configured to generate an output signal at an output node in response to an input signal received through an input node;

a bias circuit coupled between an output transistor of said Darlington transistor pair and said input node, said bias circuit comprising (a) a bias transistor, (b) a bypass capacitor, and (c) a choke resistor connected between a base of said bias transistor and base of said output transistor; and

a low noise filter implementation comprising at least one choke inductor and at least one bypass capacitor.

23. (NEW) An apparatus comprising:

a Darlington transistor pair configured to generate an output signal at an output node in response to an input signal received through an input node;

a bias circuit coupled between an output transistor of said Darlington transistor pair and said input node, said bias circuit comprising (a) a bias transistor, (b) a bypass capacitor, and (c) a resistor connected between a base of said bias transistor and base of said output transistor; and

a low noise filter implementation comprising at least one choke inductor.

24. (NEW) The apparatus according to claim 23, further comprising:

a feedback resistor coupled between said output node and said input node of said Darlington transistor pair.

25. (NEW) The apparatus according to claim 23, further comprising:

a feedback resistor coupled between a collector of bias transistor and said output node.

26. (NEW) An apparatus comprising:

a Darlington transistor pair configured to generate an output signal at an output node in response to an input signal received through an input node;

a bias circuit coupled between an output transistor of said Darlington transistor pair and said input node, said bias circuit comprising (a) a bias transistor, (b) a bypass capacitor, and (c) a resistor connected between a base of said bias transistor and base of said output transistor; and

a low noise filter implementation comprising at least one bypass capacitor.

27. (NEW) The apparatus according to claim 26, further comprising:

a feedback resistor coupled between said output node and said input node of said Darlington transistor pair.

28. (NEW) The apparatus according to claim 26, further comprising:

a feedback resistor coupled between said output node and a collector of said bias transistor.

29. (NEW) An apparatus comprising:

a Darlington transistor pair configured to generate an output signal at an output node in response to an input signal received through an input node;

a bias circuit coupled between an output transistor of said Darlington transistor pair and said input node, said bias circuit comprising (a) a bias transistor, (b) a bypass capacitor, and (c) a resistor connected between a base of said bias transistor and base of said output transistor; and

a feedback resistor coupled between said output node and said input node of said Darlington transistor pair.

30. (NEW) The apparatus according to claim 29, wherein said feedback resistor is used to set the nominal bias current of said apparatus.

31. (NEW) The apparatus according to claim 29, further comprising:

a filter coupled to a collector of said bias transistor.

32. (NEW) The apparatus according to claim 31, wherein said filter comprises at least one bypass capacitor.

33. (NEW) An apparatus comprising:

a Darlington transistor pair configured to generate an output signal at an output node in response to an input signal received through an input node;

a bias circuit coupled between an output transistor of said Darlington transistor pair and said input node, said bias circuit comprising (a) a bias transistor, (b) a bypass capacitor, and (c) a resistor connected between a base of said bias transistor and base of said output transistor; and

a feedback resistor coupled between a collector of the bias transistor and the output node.

34. (NEW) The apparatus according to claim 33, wherein said apparatus further comprises:

an isolation resistor coupled between said input node and a collector of said bias transistor, said isolation resistor configured to improve low frequency radio frequency (RF) response.

35. (NEW) A method for self-biasing a Darlington amplifier comprising the steps of:

(A) implementing a Darlington transistor pair configured to generate an output signal at an output node in response to an input signal received through an input node;

(B) coupling a bias circuit between an output transistor of said Darlington transistor pair and said input node, said bias circuit comprising (a) a bias transistor, (b) a bypass capacitor, and (c) a resistor connected between a base of said bias transistor and base of said output transistor; and

(C) implementing a low noise filter comprising at least one choke inductor and at least one bypass capacitor.

36. (NEW) The method according to claim 35, further comprising the step of:

implementing a feedback resistor coupled between said output node and said input node of said Darlington pair.

37. (NEW) The method according to claim 14, further comprising the step of:

implementing a filter comprising at least one bypass capacitor.

38. (NEW) The method according to claim 14, further comprising the step of:

implementing a filter comprising at least one choice inductor.